

the patent warranted hereon all changes and modifications as reasonably and properly come within the scope of their contribution to the art.--.

IN THE CLAIMS:

On page 8, in line 1, cancel "Patent Claims" substitute --**WE**
5 **CLAIM AS OUR INVENTION:**-- therefor.

Please cancel claims 1-10 and substitute the following claims 11-21
therefor:

11. An integrated circuit arrangement comprising:
a semiconductor substrate having at least one doped region; and
10 a plane arranged on a surface of said substrate and having a
number of conductive useful structures and at least one
conductive filler structure, said conductive filler structure
being conductively connected to said doped region.
12. The integrated circuit arrangement according to claim 11,
15 further comprising:
a planarizing insulation layer surrounding said conductive useful
structures and said conductive filler structure; and
wherein said conductive useful structures and said conductive filler
structure are essentially a same height.
13. The integrated circuit arrangement according to claim 11,
20 further comprising:
a contact connecting said conductive filler structure to said doped
region via a through hole.
14. The integrated circuit arrangement according to claim 13,
25 wherein said through hole overlaps said conductive filler structure and
said doped region exposing a surface of said conductive filler structure
and a surface of said doped region, said contact being in communication

with said surface of said conductive filler structure and said surface of said doped region.

15 15. The integrated circuit arrangement according to claim 11,
 wherein said conductive useful structures are gate electrodes; and
 5 wherein said conductive filler structure contains a material of said gate
 electrodes.

 16. The integrated circuit arrangement according to claim 11,
 wherein said doped region is a doped well in said semiconductor
 substrate.

10 17. The integrated circuit arrangement according to claim 11,
 further comprising:
 a metallization layer arranged above said plane wherein said
 conductive filler structure is arranged; and
 a further contact connecting said conductive filler structure to said
15 metallization layer.

 18. A method for manufacturing an integrated circuit
 arrangement, said method comprising the steps of:
 forming a doped region in a semiconductor substrate;
 forming a plane on a surface of said semiconductor substrate by
20 applying and structuring a conductive layer, said plane
 having a number of conductive useful structures and at least
 one conductive filler structure;
 producing an insulation layer surrounding and covering said
 conductive useful structures and said conductive filler
25 structure; and
 producing a conductive connection between said conductive filler
 structure and said doped region.

19. The method according to claim 18, wherein said step of producing a connection between said conductive filler structure and said doped region further comprises the steps of:

5 opening a through hole in said insulation layer, said through hole
 respectively partially overlapping said conductive filler
 structure and said doped region for partially uncovering a
 surface of said doped region and a surface of said
 conductive filler structure; and

10 forming a contact in said through hole, said contact being in
 communication with said surface of said conductive filler
 structure and said surface of said doped region.

20. The method according to claim 18, further comprising the steps of:

15 producing a metallization layer above said plane wherein said
 conductive filler structure is formed; and
 producing a further contact connecting said conductive filler
 structure to said metallization layer.

21. The integrated circuit arrangement according to claim 11,
wherein said doped region is said semiconductor substrate.